CLAIMS:

1. An instruction processing device comprising

- an instruction issue unit for issuing successive instructions;
- a plurality of pipe-line stages coupled to the instruction issue unit, at least one of the pipe-line stages comprising a functional unit for executing a command from the instructions;
- a first register unit coupled to the functional unit for storing a result of execution of the command when the command has reached a first one of the pipeline stages, and for supplying bypass operand data to a circuit in a pipe-line stage preceding the first one of the pipeline stages;
- a second register unit, coupled to the functional unit for storing the result when the command has reached a second one of the pipeline stages, downstream from the first one of the pipeline stages, and for supplying operand data to the functional unit;
- a disable circuit coupled to selectively disable storing of the results in the second register unit under control of the instructions.

2. An instruction processing device according to Claim 1, wherein the first and second register unit each comprise a plurality of registers and addressing circuitry for selective addressing with a register address from the command, for selecting a register for storing the result and/or for retrieving operand data.

3. An instruction processing device according to Claim 2, wherein the first register unit contains fewer registers than the second register unit.

4. An instruction processing device according to Claim 2, wherein the disable circuit is arranged to suppress a supply of clock signals to circuitry for writing the result into a register of the second register unit from a write port of the second register unit.

5. An instruction processing device according to Claim 3, comprising a plurality of functional units, arranged to execute respective commands from an instruction in parallel,

the second register unit having a plurality of write ports for writing the result from respective ones of the functional unit, the disable circuit being arranged to disable writing at selected write ports, selected under control of the instructions.

6. An instruction processing device according to Claim 2, comprising a bypass control unit arranged to compare a result register address for the result from a first one of the commands with an operand register address from a second one of the commands that follows the first one of the commands directly or indirectly, and to substitute a result from the register of the first register unit that contains the result for an operand from the second register unit in case of a match of the addresses.

7. An instruction processing device according to Claim 1, wherein the first register unit comprises a chain of registers for supplying bypass operand data, arranged as a shift register with an input coupled to a result output of the first one of the stages and operative to shift the result through successive shift register stages in successive instruction cycles, at least if storing of the result in the second register unit is disabled, the chain extending further than necessary for writing the result into the second register unit.

8. An instruction processing device according to Claim 7, wherein the registers in the chain are addressable from the commands.

9. An instruction processing device according to Claim 2, comprising a plurality of functional units, arranged to execute respective commands from an instruction in parallel, the first register unit comprising respective groups of registers, each for storing results from a respective one of the functional units only, the registers of all groups being addressable from the command for retrieving an operand.

10. A method of executing a program of instructions in an instruction processor, the method comprising

- pipelining execution of commands from the instructions;
- in the absence of instruction to the contrary storing results of the commands in a register file;
- in the absence of instruction to the contrary retrieving register sourced operands of the commands from the register file;

- selectively using a first one of the results bypassed from a pipelining stage as a bypassed operand instead of at least one of the register sources operands from the register file;
- selectively suppressing, under program control, writing of the first one of the results to the register file.

11. A method according to Claim 10, comprising writing the first one of the results into an addressable one of a plurality of bypass registers that are located to receive the result earlier during pipelining than the register file.

12. A computer program product comprising instructions for an instruction processor for implementing the method according to Claim 10 or 11.

13. A method of compiling a program of instructions for an instruction processor, the method comprising
- generating a series of instructions;
- first detecting for a result to be produced by a first one of the instructions which second one of the instructions use the result as operand;
- second detecting whether it can be guaranteed that it will be possible to bypass the result in the instruction processor as operand for all second ones of the instructions without retrieving the result from a register file;
- generating information in the instruction to disable writing to the register file when it can be guaranteed that it will be possible to bypass the result as operand in the instruction processor for all second ones of the instructions.

14. A method of compiling according to Claim 12, comprising including an indication in the instructions that the result should be stored in one of a plurality of bypass registers that is addressable on writing and/or reading of the result to the plurality of bypass registers.

15. A computer program product comprising instructions for an instruction processor for implementing the method according to Claim 13 or 14.